OIPE IAP15 JUL 3 1 2006 PATENT & TRADEMARK OFFICE

Docket No.: 0756-7181

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)
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Application No.: 10/625,904	) Examiner: Ahmed N. Sefer
Filed: July 24, 2003	) Group Art Unit: 2826
For: SEMICONDUCTOR DEVICE AND	)
METHOD OF FABRICATING THE	)
SAME	)

VERIFICATION OF TRANSLATION

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Sir:

I, Satomi Hata, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, herewith declare:

that I am well acquainted with both the Japanese and English Languages; and

that to the best of my knowledge and belief the following is a true and correct English translation of the Japanese Patent Application No. 11-231281 filed on August 18, 1999.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 14th day of July 2006

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[Name of Document] Patent Application
[Reference Number] P004310-06
[Filing Date] August 18th, 1999
[Attention] Commissioner, Patent Office Takeshi ISAYAMA
[International Patent Classification] H01L 21/00

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[Indication of Handlings]
[Number of Prepayment Note] 002543
[Payment Amount] ¥21,000
[List of Attachment]
[Attachment] Specification 1
[Attachment] Drawing 1
[Attachment] Abstract 1
[Proof] Required

[Name of Document] Specification

[Title of the Invention]
SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

[Scope of Claim]
[Claim 1]
A semiconductor device comprising:
a base film comprising a region with a first thickness and a region with a second thickness thinner than the first thickness, and the region with the first thickness has a smaller area than the region with the second thickness; and
an island-shaped semiconductor layer having a crystal structure over the base film, the island-like semiconductor layer is formed over the region with the first thickness and the region with the second thickness.

[Claim 2]
A semiconductor device comprising a thin film transistor over a translucent substrate,

wherein a base film having a region with a first thickness and a region with a second thickness thinner than the first thickness is provided over one surface of the translucent substrate;

wherein the region with the first thickness has a smaller area than the region with the second thickness; and

at least a part of a channel formation region of the thin film transistor is provided over the region with the first thickness.

[Claim 3]

A semiconductor device according to claim 1 or 2, wherein a difference in film thickness between the region with the first thickness and the region with the second thickness is 50 to 100 nm.

[Claim4]

A semiconductor device comprising:

a heat conduction layer formed in an island-shape over one surface of a translucent substrate,

wherein a base film over the translucent substrate is formed so as to cover the heat conduction layer; and

wherein an island-shaped semiconductor layer having a crystal structure over the base film has at least a part formed over the heat conduction layer.

[Claim 5]

A semiconductor device comprising a thin film transistor over a translucent substrate,

wherein the heat conduction layer formed in an island-shape over one surface of a translucent substrate;

wherein a base film over the translucent substrate is formed so as to cover the heat conduction layer; and

wherein a channel forming region of the thin film transistor has at least a part formed over the heat conduction layer.

[Claim 6]

A semiconductor device according to claim 4 or 5.

wherein the heat conduction layer is formed of one or a plurality selected from aluminum oxide, aluminum nitride, and aluminum oxynitride.

[Claim 7]

A semiconductor device according to claim 4 or 5,

wherein the heat conduction layer is formed of a compound comprising Si, N, O and M (M is at least one selected from Al or a rare earth element).

[Claim 8]

A method of fabricating a semiconductor device, comprising the steps of:

forming a base film with a first thickness over one surface of a translucent substrate;

forming a region with the first thickness and a region with a second thickness thinner than the first thickness by etching a part of the base film;

forming an island-shaped semiconductor layer over the base film and over the region with the first thickness and the region with the second thickness; and

crystallizing the island-shaped semiconductor layer by irradiating the island-shaped semiconductor layer with a laser beam from one surface side and the other surface side of the translucent substrate.

[Claim 9]

A method of fabricating a semiconductor device in which a thin film transistor is provided over a translucent substrate, comprising the steps of:

forming a base film with a first thickness over one surface of the translucent substrate;

forming a region with the first thickness and a region with a second thickness thinner than the first thickness by etching a part of the base film;

forming an island-shaped semiconductor layer over the base film and over the region with the first thickness and the region with the second thickness;

crystallizing the island-shaped semiconductor layer by irradiating the island-shaped semiconductor layer with a laser beam from one surface side and the other surface side of the translucent substrate; and

forming the thin film transistor so that at least a part of a gate electrode of the thin film transistor overlaps with the region with the first thickness.

[Claim 10]

A method of manufacturing a semiconductor device, according to claim 8 or 9,

wherein a difference in film thickness between the region with the first thickness and the region with the second thickness is 50 to 100 nm.

[Claim 11]

A pulse output circuit according to any one of claims 1 to 7,

wherein the laser beam irradiated to the island-shaped semiconductor layer from the other surface side is a laser beam which has passed through the translucent substrate.

[Claim 12]

A method of fabricating a semiconductor device, comprising the steps of:

forming an island-shaped heat conduction layer over one surface of a translucent substrate;

forming a base film with a first thickness over the translucent substrate to cover the island-like heat conduction layer;

forming an island-shaped semiconductor layer which is formed over the base film, which has an area larger than the island-shaped heat conduction layer, and at least a part of which overlaps with the island-shaped heat conduction layer; and

crystallizing the island-shaped semiconductor layer by irradiating the island-shaped semiconductor layer with a laser beam from one surface side and the other surface side of the translucent substrate.

[Claim 13]

A method of fabricating a semiconductor device in which a thin film transistor is formed

over a translucent substrate, comprising the steps of:

forming an island-shaped heat conduction layer over one surface of a translucent substrate;

forming a base film with a first thickness over the translucent substrate to cover the island-like heat conduction layer;

forming an island-shaped semiconductor layer which is formed over the base film, which has an area larger than the island-shaped heat conduction layer, and at least a part of which overlaps with the island-shaped heat conduction layer;

crystallizing the island-shaped semiconductor layer by irradiating the island-shaped semiconductor layer with a laser beam from one surface side and the other surface side of the translucent substrate; and

forming the thin film transistor so that at least a part of a gate electrode of the thin film transistor overlaps with the island-shaped heat conduction layer.

[Claim 14]

A method of fabricating a semiconductor device according to claim 12 or 13,

wherein the island-shaped heat conduction layer is formed of at least one selected from aluminum oxide, aluminum nitride, and aluminum nitride oxide.

[Claim 15]

A method of fabricating a semiconductor device according to claim 12 or 13,

wherein the heat conduction layer is formed of a compound containing Si, N, O and M, (M is at least one selected from Al or a rare earth element).

[Claim 16]

A method of fabricating a semiconductor device, comprising the steps of:

forming a base film with a first thickness over one surface of a translucent substrate;

forming a region with the first thickness and a region with a second thickness thinner than the first thickness by etching a part of the base film;

forming an island-shaped semiconductor layer over the base film and over the region of the first thickness and the region of the second thickness; and

crystallizing the island-shaped semiconductor layer by irradiating one surface side of the translucent substrate with a laser beam and by causing a reflecting plate provided on the other surface side of the translucent substrate to reflect the laser beam, which was incident over a peripheral region of the island-shaped semiconductor layer and passed through the translucent substrate, so that the laser beam is irradiated from the other surface side of the translucent substrate.

[Claim 17]

A method of fabricating a semiconductor device in which a thin film transistor is provided over a translucent substrate, comprising the steps of:

forming a base film with a first thickness over one surface of a translucent substrate;

forming a region with the first thickness and a region with a second thickness thinner than the first thickness by etching a part of the base film;

forming an island-shaped semiconductor layer over the base film and over the region of the

first thickness and the region of the second thickness; and

crystallizing the island-shaped semiconductor layer by irradiating one surface side of the translucent substrate with a laser beam and by causing a reflecting plate provided on the other surface side of the translucent substrate to reflect the laser beam, which was incident over a peripheral region of the island-shaped semiconductor layer and passed through the translucent substrate, so that the laser beam is irradiated from the other surface side of the translucent substrate; and

forming the thin film transistor so that at least a part of a gate electrode of the thin film transistor overlaps with the island-shaped heat conduction layer.

[Claim 18]

A method of fabricating a semiconductor device, comprising the steps of:

forming an island- shaped heat conduction layer over one surface of a translucent substrate;

forming a base film with a first thickness over the translucent substrate to cover the island-shaped heat conduction layer;

forming an island-shaped semiconductor layer which is formed over the base film, which has an area larger than the island-shaped heat conduction layer, and at least a part of which overlaps with the island-shaped heat conduction layer; and

crystallizing the island-shaped semiconductor layer by irradiating one surface side of the translucent substrate with a laser beam and by causing a reflecting plate provided at the other surface side of the translucent substrate to reflect the laser beam, which was incident over a peripheral region of the island-shaped semiconductor layer and passed through the translucent substrate, so that the laser beam is irradiated from the other surface side of the translucent substrate.

[Claim 19]

A method of fabricating a semiconductor device in which a thin film transistor is provided over a translucent substrate, comprising the steps of:

forming an island- shaped heat conduction layer over one surface of a translucent substrate;

forming a base film with a first thickness over the translucent substrate to cover the island-shaped heat conduction layer;

forming an island-shaped semiconductor layer which is formed over the base film, which has an area larger than the island-shaped heat conduction layer, and at least a part of which overlaps with the island-shaped heat conduction layer; and

crystallizing the island-shaped semiconductor layer by irradiating one surface side of the translucent substrate with a laser beam and by causing a reflecting plate provided at the other surface side of the translucent substrate to reflect the laser beam, which was incident over a peripheral region of the island-shaped semiconductor layer and passed through the translucent substrate, so that the laser beam is irradiated from the other surface side of the translucent substrate.

[Claim 20]

A method of fabricating a semiconductor device according to any one of claims 16 to 19,

wherein reflectivity of the reflecting plate is 20 to 90%.

[Claim 21]

A method of fabricating a semiconductor device according to claim 16 or 17, wherein a difference in film thickness between the region with the first thickness and the region with the second thickness is 50 to 100 nm.

[Claim 22]

A method of fabricating a semiconductor device according to claim 18 or 19, wherein the island-shaped heat conduction layer is formed of at least one selected from aluminum oxide, aluminum nitride, and aluminum nitride oxide.

[Claim 23]

A method of fabricating a semiconductor device according to claim 18 or 19, wherein the heat conduction layer is formed of a compound containing Si, N, O and M (M is at least one selected from Al or a rare earth element).

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention relates to a method of fabricating a semiconductor film having a crystal structure and formed on a substrate having an insulating surface, and a method of fabricating a semiconductor device using the semiconductor film as an active layer. Particularly, the present invention relates to a method of fabricating a thin film transistor in which an active layer is formed of a crystalline semiconductor layer. Incidentally, in the present specification, the term "semiconductor device" indicates all devices capable of functioning by using semiconductor characteristics, and includes, in its category, an electro-optical device typified by an active matrix type liquid crystal display device formed by using thin film transistors, and an electronic equipment incorporating that kind of electro-optical device as a part.

[0002]

[Prior Art]

There has been developed a thin film transistor (hereinafter referred to as a TFT) in which an amorphous semiconductor layer is formed on a translucent substrate having an insulating surface and a crystalline semiconductor layer crystallized by a laser annealing method, a thermal annealing method or the like is made an active layer. As the insulating substrate, a glass substrate of barium borosilicate glass or alumino borosilicate glass is often used. Although such a glass substrate is inferior to a quartz substrate in heat resistance, it has merits in that its market price is inexpensive and a large area substrate can be easily manufactured.

[0003]

The laser annealing method is known as a crystallizing technique in which it is possible to crystallize an amorphous semiconductor layer by giving high energy to only the amorphous semiconductor layer without raising the temperature of a glass substrate very much. Particularly an excimer laser capable of obtaining short wavelength light having a wavelength of 400 nm or less and large output is regarded as most suitable in this usage. The laser annealing method using the

excimer laser is carried out in such a manner that a laser beam is processed by an optical system into a spot shape or a linear shape on a surface to be irradiated, and the surface to be irradiated on the substrate is scanned by the processed laser light (irradiation position of the laser light is moved relatively to the surface to be irradiated). For example, in an excimer laser annealing method using linear laser light, it is also possible to make laser annealing of all the surfaces to be irradiated by scanning only in the direction perpendicular to its longitudinal direction, and is superior in productivity, so that it has become the mainstream of a manufacturing technique of a liquid crystal display device using TFTs. The technique enables a monolithic type liquid crystal display device in which TFTs (pixel TFTs) for forming a pixel portion and TFTs of a driving circuit provided at the periphery of the pixel portion are formed on one glass substrate.

[0004]

However, a crystalline semiconductor layer fabricated by the laser annealing method is formed of an aggregation of plural crystal grains, and the positions and sizes of the crystal grains are random. TFTs fabricated on the glass substrate are formed such that the crystalline semiconductor layer is separated into an island-like pattern for the purpose of element separation. In that case, it was impossible to form the crystal grains by specifying the positions and sizes of them. In the interface (crystal grain boundary) of the crystal grain, there is a cause to lower current transport characteristics of carriers because of a recombination center or trapping center due to an amorphous structure, crystal defect or the like, or the influence of a potential level at the crystal grain boundary. However, it has been hardly possible to form a channel formation region, in which the property of a crystal greatly influences the characteristics of a TFT, by a single crystal grain so as to exclude the influence of the crystal grain boundary. Thus, a TFT including an active layer of a crystalline silicon film and having characteristics comparable to those of a MOS transistor has not been obtained till today.

[0005]

In order to solve such problems, an attempt to grow a large crystal grain has been made. For example, in "High-Mobility Poly-Si Thin-Film Transistors Fabricated by a Novel Excimer Laser Crystallization Method", K. Shimizu, O. Sugiura, and M. Matumura, IEEE Transactions on Electron Devices vol. 40. No. 1, pp 112-117, 1993, there is a report on a laser annealing method in which a film of three-layer structure of $Si/SiO_2/Si$ is formed on a substrate, and excimer laser light is irradiated from both sides of a film side and a substrate side. This report discloses that according to this method, the size of a crystal grain can be enlarged by irradiation of laser light at predetermined energy intensity.

[0006]

[Problems to be solved by the Invention]

The above-mentioned method of Ishihara et al. is characterized in that heat characteristics of a base material of an amorphous silicon film are locally changed and the flow of heat to the substrate is controlled, so that a temperature gradient is caused. However, for that purpose, the three-layer structure of high melting point metal layer/silicon oxide layer/semiconductor film is formed on the glass substrate. Although it is possible to form a top gate type TFT by using the semiconductor film as an active layer in view of structure, since parasitic capacitance is generated by the silicon oxide film provided between the semiconductor film and the high melting point metal layer, power consumption is increased and it becomes

difficult to realize high speed operation of the TFT.

[0007]

On the other hand, when the high melting point metal layer is made a gate electrode, it is conceivable that the method can be effectively applied to a bottom gate type or reverse stagger type TFT. However, in the foregoing three-layer structure, even if the thickness of the semiconductor film is omitted, with respect to the thickness of the high melting point metal layer and the silicon oxide layer, since the thickness suitable for a crystallizing step is not necessarily coincident with the thickness suitable for the characteristics as a TFT element, it is impossible to simultaneously satisfy both the optimum design in the crystallizing step and the optimum design in the element structure.

[0008]

Besides, when the opaque high melting point metal layer is formed on the entire surface of the glass substrate, it is impossible to fabricate a transmission type liquid crystal display device. Although the high melting point metal layer is useful in that its thermal conductivity is high, since a chromium (Cr) film or titanium (Ti) film used as the high melting point metal material layer has high internal stress, there is a high possibility that a problem as to adhesiveness to the glass substrate occurs. Further, the influence of the internal stress is also exerted on the semiconductor film formed as the upper layer, and there is a high possibility that the stress functions as force to impart distortion to the formed crystalline semiconductor film.

[0009]

On the other hand, in order to control a threshold voltage (hereinafter referred to as Vth) as an important characteristic parameter in a TFT within a predetermined range, in addition to valence electron control of the channel formation region, it is necessary to reduce the charged defect density of a base film and a gate insulating film formed of an insulating film to be in close contact with the active layer, or to consider the balance of the internal stress. To such requests, a material containing silicon as its constituent element, such as a silicon oxide film or a silicon nitride oxide film, has been suitable. Thus, there is a fear that the balance is lost by providing the high melting point metal layer to cause the temperature gradient.

[0010]

The present invention has been made to solve such problems, and an object of the invention is to realize a TFT capable of operating at high speed by fabricating a crystalline semiconductor film in which the positions and sizes of crystal grains are controlled and further by using the crystalline semiconductor film for a channel formation region of the TFT. Further, another object of the invention is to provide a technique enabling such a TFT to be applied to various semiconductor devices such as a transmission type liquid crystal display device or a display device using organic electroluminescence material.

[0011]

[Means for Solving the Problems]

A laser annealing method is used as a method of forming a crystalline semiconductor layer from an amorphous semiconductor layer formed on a substrate of glass or the like. In the laser annealing method of this invention, a pulse oscillation or continuous-wave excimer laser or argon laser is used as a light source, and laser light formed into a linear shape by an optical system is irradiated to an island-like semiconductor layer from both sides of a front side of a substrate where the island-shaped semiconductor layer is formed (in this specification, the front side is defined as a

surface where an island-shaped semiconductor layer is formed) and a reverse side (in this specification, it is defined as a surface opposite to the surface where the island- shaped semiconductor layer is formed).

[0012]

FIG. 2A is a view showing a structure of a laser annealing apparatus of the present invention. The laser annealing apparatus includes a laser oscillator 1201, an optical system 1100, and a stage 1202 for fixing a substrate. The stage 1202 is provided with a heater 1203 and a heater controller 1204, and can heat the substrate up to 100 to 450°C. A reflecting plate 1205 is provided on the stage 1202, and a substrate 1206 is set thereon. In the structure of the laser annealing apparatus of FIG. 2A, a method of holding the substrate 1206 will be described with reference to FIG. 2B. The substrate 1206 held at the stage 1202 is set in a reaction chamber 1213, and is irradiated with laser light. The inside of the reaction chamber can be made a low pressure state or inert gas atmosphere by a not-shown exhaust system or gas system, and a semiconductor film can be heated up to 100 to 450°C without pollution. The stage 1202 can be moved along a guide rail 1216 in the reaction chamber, and the entire surface of the substrate can be irradiated with the linear laser light. The laser light is incident from a not-shown quartz window provided above the substrate 1206. Besides, in FIG. 2B, a transfer chamber 1210, an intermediate chamber 1211, and a load/unload chamber 1212 are connected to the reaction chamber 1213, and they are separated by partition valves 1217 and 1218. A cassette 1214 capable of holding a plurality of substrates is set in the load/unload chamber 1212, and the substrate is conveyed by a conveying robot 1215 provided in the transfer chamber 1210. A substrate 1206' indicates a substrate under conveyance. By adopting such structure, it is possible to continuously carry out laser annealing under the low pressure or in the inert gas atmosphere.

[0013]

FIGS. 3A and 3B are views for explaining the structure of the optical system 1100 of the laser annealing apparatus shown in FIG. 2A. An excimer laser, an argon laser, or the like is used as a laser oscillator 1101. FIG. 3A is a view of the optical system 1100 seen from the side, and laser light emitted from the laser oscillator 1101 is divided in the vertical direction by a cylindrical lens array 1102. After the divided laser light is once condensed by a cylindrical lens 1104, it broadens, is reflected by a mirror 1107, and then, is made linear laser light on an irradiation surface 1109 by a cylindrical lens 1108. By this, the energy distribution of the linear laser beam in a width direction can be uniformed. FIG. 3B is a view of the optical system 1100 seen from above, and the laser light emitted from the laser oscillator 1101 is divided in the horizontal direction by the cylindrical lens array 1102. Thereafter, the laser beams are synthesized into one beam on the irradiation surface 1109 by the cylindrical lens 1105. By this, the energy distribution of the linear laser beam in the longitudinal direction can be uniformed.

[0014]

FIG. 1 is a view for explaining the concept of a laser annealing method of the present invention. An insulating film 1002 is formed on a substrate 1001 of glass or the like, and an island-like semiconductor layer 1003 is formed thereon. A silicon oxide film, a silicon nitride film, a silicon nitride oxide film, an insulating film containing aluminum as its main ingredient, or the like is applied to the insulating film 1002, and a single film among these or a suitable combination of these is used. By the optical system explained in FIGS. 3A and 3B, the laser beam having

passed through the cylindrical lens 1005 with the function equivalent to the cylindrical lens 1108 is irradiated as the linear laser beam to the island-like semiconductor layer 1003. The island-like semiconductor layer 1003 receives a first laser light component 1006 which passes through the cylindrical lens 1005 and is directly irradiated to the island-like semiconductor layer 1003 and a second laser beam component 1007 which passes through the insulating film 1002 and the substrate 1001, is reflected by a reflecting plate 1004, again passes through the substrate 1001 and the insulating film 1002, and is irradiated to the island-like semiconductor layer 1003. In any case, since the laser light having passed through the cylindrical lens 1005 has an incident angle of 45 to 90° with respect to the surface of the substrate in the condensing process, the laser light reflected by the reflecting plate 1004 is also reflected toward the inside of the island-like semiconductor layer 1003. In the reflecting plate 1004, a reflecting surface is formed of aluminum (Al), titanium (Ti), titanium nitride (TiN), chromium (Cr), tungsten (W), tungsten nitride (WN), or the like. Like this, by suitably selecting the material forming the reflecting surface, the reflectivity can be changed in the range of 20 to 90%, and the intensity of the laser light incident from the reverse side of the substrate 1001 can be changed. If the reflection surface is made a mirror surface, positive reflectivity of about 90% can be obtained within the wavelength range of 240 to 320 nm. Besides, if the material is made aluminum and minute uneven shapes of several hundred nm are formed on the surface, diffusion reflectivity (integral reflectivity - positive reflectivity) of 50 to 70% is obtained.

[0015]

In this way, the laser beam is irradiated from the front surface and the reverse surface of the substrate 1001, and the island-like semiconductor layer formed on this substrate 1001 is laser annealed from both surfaces. In the laser annealing method, by optimizing the condition of irradiated laser light, a semiconductor film is instantaneously heated and melted, and the generation density of crystal nuclei and crystal growth from the crystal nuclei is controlled. Since the oscillation pulse width of an excimer laser is several nano seconds to several tens nano seconds, for example, 30 nano seconds, if irradiation is made under a pulse oscillation frequency of 30 Hz, the semiconductor layer of the region which is irradiated with the laser light is instantaneously heated by the pulse laser light, and is cooled for a time far longer than the heating time.

[0016]

If the laser beam is irradiated to the island-like semiconductor layer formed on the substrate from only one surface, only one side is heated, so that a cycle of heating melting and cooling solidification becomes steep. Thus, even if the generation density of crystal nuclei can be controlled, satisfactory crystal growth can not be expected. However, if the laser beam is irradiated from both surfaces of the semiconductor layer, the cycle of heating melting and cooling solidification becomes gentle, and a time allowed for crystal growth in the process of cooling solidification becomes relatively long, so that satisfactory crystal growth can be obtained.

[0017]

In the transient phenomenon, an attempt is made such that the island-like semiconductor layer is made to have a temperature distribution, a region where temperature change is gentle is formed, and a nucleus generation speed and nucleus generation density are controlled, so that the size of the crystal grain is enlarged. Specifically, as shown in FIG. 1, in the region where the island-like semiconductor layer 1003 overlaps with the base film 1002, a thick portion is formed in

the base film 1002. At this portion, since its volume is increased and heat capacity is increased, the cycle of temperature change of the island-like semiconductor layer by the irradiation of the pulse laser beam becomes gentle (as compared with the other thin portion). In the present invention, like this, the substrate is irradiated with the laser light from the front surface side and the reverse surface side to directly heat the semiconductor layer, and at the same time, heat conduction control from the semiconductor layer to the substrate side and heat conduction (due to a temperature gradient) of the semiconductor layer in the horizontal direction to the substrate are used, so that enlargement of the size of the crystal grain is realized.

[0018]

In addition, with respect to the method of irradiating the substrate on which the island-like semiconductor layer is formed with the laser beam from the front surface side and the reverse surface side thereof, a structure shown in FIG. 4 may be used. Light emitted from a laser oscillator 401 such as an excimer laser is divided by a cylindrical lens array 402 (or 403). After this divided laser light is once condensed by a cylindrical lens 404 (or 405), it broadens and is reflected by a mirror 408. A beam splitter 406 is put on the midway of this optical path to divide the optical path in two. One laser light is reflected by mirrors 407 and 413, is made linear laser light by a cylindrical lens 414, and irradiated to the front side of a substrate 418. This laser light is made first laser light. A base film 419 and an island-like semiconductor layer 420 are formed on the front side of the substrate 418. The other laser light is reflected by mirrors 408, 409 and 411, is made linear laser light by a cylindrical lens 412, and is irradiated to the reverse side of the substrate 418. This laser light is made second laser light. In the midway of this optical path, an attenuator is provided to adjust the intensity of the laser light. In this structure, even when the substrate is irradiated with the laser light from the front side and the reverse side thereof, the size of the crystal grain of the semiconductor layer can be enlarged similarly to the foregoing.

[0019]

In this invention, such a laser annealing method is called a dual beam laser annealing method, and this method is used to enlarge the size of a crystal grain of an island-like semiconductor layer. Such an island-like semiconductor layer is used for an active layer of a TFT, and further, a semiconductor device including a TFT having a structure in accordance with the function of each circuit is fabricated, so that the performance of the semiconductor device is improved.

[0020]

The structure of the present invention using such a dual beam laser annealing method is characterized in that a base film having a region with a first thickness and a region with a second thickness smaller than the first thickness are formed on one surface of a translucent substrate, the region with the first thickness has an area smaller than the region with the second thickness, and an island-like semiconductor layer having a crystal structure on the base film is formed over the region with the first thickness and the region with the second thickness.

[0021]

Another structure of the invention is characterized in that a heat conduction layer formed like an island is provided on one surface of a translucent substrate, a base film on the translucent substrate is formed to cover the heat conduction layer, and at least a part of an island-like semiconductor layer having a crystal structure on the base film is formed on the heat conduction layer.

[0022]

Besides, another structure of the present invention is characterized by including a step of forming a base film with a first thickness on one surface of a translucent substrate, a step of forming a region with the first thickness and a region with a second thickness smaller than the first thickness by etching a part of the base film, a step of forming an island-like semiconductor layer on the base film and over the region with the first thickness and the region with the second thickness, and a step of crystallizing the island-like semiconductor layer by irradiating the island-like semiconductor layer with laser light from one surface side and the other surface side of the translucent substrate.

[0023]

Besides, another structure of the present invention is characterized by including a step of forming an island-like heat conduction layer on one surface of a translucent substrate, a step of forming a base film of a first thickness on the translucent substrate to cover the island-like heat conduction layer, a step of forming an island-like semiconductor layer which is formed on the base film, which has an area larger than the island-like heat conduction layer, and at least a part of which overlaps with the island-like heat conduction layer, and a step of crystallizing the island-like semiconductor layer by irradiating the island-like semiconductor layer with laser light from one surface side of the translucent substrate and the other surface side.

[0024]

Besides, another structure of the present invention is characterized by including a step of forming a base film with a first thickness on one surface of a translucent substrate, a step of forming a region with a first thickness and a region with a second thickness smaller than the first thickness by etching a part of the base film, a step of forming an island-like semiconductor layer on the base film and over the region with the first thickness and the region with the second thickness, and a step of crystallizing the island-like semiconductor layer by irradiating laser light from one surface side of the translucent substrate and by causing a reflecting plate provided at the other surface side of the translucent substrate to reflect the laser light, which was incident on a peripheral region of the island-like semiconductor layer and passed through the translucent substrate, so that the laser light is irradiated from the other surface side of the translucent substrate.

[0025]

Besides, another structure of the present invention is characterized by including a step of forming an island-like heat conduction layer on one surface of a translucent substrate, a step of forming a base film of a first thickness on the translucent substrate to cover the island-like heat conduction layer, forming an island-like semiconductor layer which is formed on the base film, which has an area larger than the island-like heat conduction layer, and at least a part of which overlaps with the island-like heat conduction layer, and a step of crystallizing the island-like semiconductor layer by irradiating laser light from one surface side of the translucent substrate and by causing a reflecting plate provided at the other surface side of the translucent substrate to reflect the laser light, which was incident on a peripheral region of the island-like semiconductor layer and passed through the translucent substrate, so that the laser light is irradiated from the other surface side of the translucent substrate.

[0026]

[Embodiment Modes of the Invention]

[Embodiment Mode 1]

An embodiment mode of the present invention will be described with reference to FIGS. 5A to 5C. In FIG. 5A, an alkali-free glass substrate of barium borosilicate glass, alumino borosilicate glass, or the like is used as a substrate 501. For example, #7059 glass or #1737 glass of Corning Inc. can be preferably used. In addition, a plastic substrate having no optical anisotropy, such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN), or polyethersulfone (PES), can also be used. On a surface of the substrate 501 on which an island-like semiconductor layer is formed, in order to prevent the diffusion of an impurity such as an alkaline metal element from the substrate 501, a base film 502 of a silicon oxide film, a silicon nitride film, or a silicon nitride oxide film is formed with a thickness of 100 to 300 nm. The base film 502 may be formed of one layer among these films, or may be formed by laminating the plurality of films. For example, a silicon nitride oxide film made from SiH_4, NH_3, and N_2O is formed by a plasma CVD method.

[0027]

In order to form a thick portion and a thin portion in this base film 502, a resist mask is formed by a photolithography technique, and an etching process is performed. As the etching, wet etching using a solution containing hydrofluoric acid, dry etching using CF_4, or the like can be applied. In any event, etching of a portion with a thickness of 30 to 100 nm is performed to partially change the thickness of the base film 502. FIG. 5A schematically shows the shape.

[0028]

Next, an amorphous semiconductor layer 503 having a thickness of 25 to 80 nm (preferably 30 to 60 nm) and an amorphous structure is formed by a well-known method such as a plasma CVD method or a sputtering method. For example, the amorphous silicon film having a thickness of 55 nm is formed by the plasma CVD method. A semiconductor film having an amorphous structure includes an amorphous semiconductor layer and a microcrystalline semiconductor film, and a compound semiconductor film having an amorphous structure, such as an amorphous silicon germanium film may be applied. Then, as shown in FIG. 5B, an island-like semiconductor layer 504 is formed from the amorphous semiconductor layer 503. The island-like semiconductor layer 504 can be made square, rectangular, or arbitrarily polygonal.

[0029]

Next, as shown in FIG. 5C, crystallization is performed by the dual beam laser annealing method. The structure and concept of its apparatus is applied similarly to that explained in FIGS. 2 to 4 as described above. For crystallization, first, it is desirable that hydrogen contained in the amorphous semiconductor layer is eliminated in advance, and it is appropriate that a heat treatment at 400 to 500°C for about 1 hour is carried out to make the hydrogen content 5 atomic% or less.

[0030]

Although the laser annealing condition is suitably selected by a user, for example, a pulse oscillation frequency of an excimer laser is made 30 Hz, a laser energy density is made 100 to 500 mJ/cm^2 (typically 300 to 350 mJ/cm^2), and a linear beam 505 with a line width of 100 to 1000 μm, for example, a line width 400 μm is irradiated. This line width is made larger than the island-like semiconductor layer 504, so that it is possible to irradiate the entire surface of at least one island-like semiconductor layer 504 at a side opposite to a substrate side and the periphery of the island-like semiconductor layer 504 by the linear beam of one pulse. A part of light irradiated to the periphery of the island-like semiconductor layer 504 at an incident angle reaches a reflecting plate placed below the substrate, and a part of light reflected at a reflection angle θ' is irradiated to

the surface of the island-like semiconductor layer 504 at the substrate side. By using such a linear beam, the same place is repeatedly irradiated. Alternatively, irradiation is made plural times while the linear beam is scanned. It is appropriate that an overlap ratio of the linear beams at this time is made 50 to 98%. Actually, it is appropriate that the number of irradiation pulses is made 10 to 40. The shape of the laser beam is not limited to the linear shape, but even if a plane shape is adopted, the same process can be made.

[0031]

In the laser annealing method like this, the light irradiated to the periphery of the island-like semiconductor layer 504 at the incident angle θ is attenuated by about 50% in the process of passing through the substrate 501. Even if the positive reflectivity of the reflecting plate is made 90%, it appears that the laser light irradiated to the surface of the island-like semiconductor layer 504 at the substrate side is about 15 to 40% of the first laser light. However, the island-like semiconductor layer 504 can be sufficiently heated even by the second laser light of such intensity. As a result, it becomes possible to sufficiently accomplish crystal growth. Since the substrate can be heated up to 100 to 450°C also by the heater 1203 provided in the stage 1202 shown in FIG. 2, an effect obtained by heating the island-like semiconductor layer can be obtained to some degree. However, heating of the semiconductor layer by the second laser beam has an effect greater than this temperature.

[0032]

In order to make the second laser light effectively incident on the center side of the island-like semiconductor layer 504, it is effective that the reflecting plate is made aluminum, minute uneven shapes of several hundreds nm are formed on the surface, and diffusion reflectivity is made 50 to 70% in advance. This is because a diffusion angle of the laser light becomes large by the surface of the minute uneven shapes.

[0033]

FIG. 5C shows the state where the first laser light 505 and the second laser light 506 are irradiated to the island-like semiconductor layer. The island-like semiconductor layer can be divided into the thick region (region A) of the base film 502 and the thin region (region B) thereof. In any case, the island-like semiconductor layer is heated by irradiation of the laser light and is put in melted state. Although it is presumed that a crystal nucleus is generated in a cooling process where the melted state is shifted to a solid phase state, the nucleus generation density correlates with the temperature and cooling speed of the melted state, and a tendency that the nucleus generation density becomes high when the melted state is rapidly cooled from high temperature has been obtained as empirical knowledge.

[0034]

When a presumption is made on the basis of such knowledge, in the region B where the melted state is rapidly cooled, the generation density of crystal nuclei becomes higher than the region A, and the crystal nuclei are generated at random, so that many crystal grains are apt to be formed, and the size of a grain becomes small by the mutual operation of the crystal grains grown from the respective crystal nuclei. On the other hand, in the region A, since the heat capacity is relatively large as compared with the region B, the temperature also becomes low. As a result, heat diffusion in the horizontal direction to the substrate surface occurs from the region B to the region A, the temperature change in the region A becomes gentle, and crystal growth is sufficiently

accomplished. At this time, by making the nucleus generation density of the region A low, the size of the crystal grain can be enlarged. From this, it is appropriate that the size of the region A is made about 2 to 6 μm. Besides, such an effect becomes remarkable when the number of repeated pulses of the irradiated pulse laser light is increased.

[0035]

As a result, as shown in FIG. 5C, in an island-like semiconductor layer 507 made of a crystalline semiconductor film, a large grain of 2 μm or more is obtained with respect to the crystal grain in the region A, and in the region B, a small crystal grain as compared with that is formed. FIG. 6 is a top view showing this state, and an island-like semiconductor layer 601 can be divided into a region A602 (inside of a square dotted line at the center portion) and a region B606 other than that. The crystal growth proceeds toward the end portion of the island-like semiconductor layer 601, with a nucleus generation region 603 in the region A602 being as the center. The distance from the center of a crystal growth end 605 can be made 1 μm or more (in FIG. 6, although it is schematically shown as a circle, an actual shape is arbitrary).

[0036]

In a subsequent step, the island-like semiconductor layer 507 is subjected to a heat treatment at 300 to 450°C in an atmosphere containing hydrogen of 3 to 100% or a heat treatment at 200 to 450°C in an atmosphere containing hydrogen generated by plasma, so that remaining defects can be neutralized. When an active layer of a TFT is fabricated while the portion of the region A of the island-like semiconductor layer 507 fabricated in this way is made a channel formation region, the characteristics of the TFT can be improved.

[0037]

[Embodiment Mode 2]

A method of fabricating an island-like semiconductor layer having a crystal structure which is made an active layer of a TFT is not limited to only a laser annealing method, but both the laser annealing method of the present invention and a thermal annealing method may be used. Particularly, when crystallization by the thermal annealing method is applied to a crystallizing method using a catalytic element disclosed in Japanese Patent Unexamined Publication No. Hei. 7-130652, crystallization can be realized at a temperature of 600°C or lower. When a crystalline semiconductor layer fabricated in this way is processed by the laser annealing method of the present invention, a crystalline semiconductor layer of high quality can be obtained. This embodiment mode will be described with reference to FIGS. 7A to 7D.

[0038]

In FIG. 7A, the glass substrate shown in Embodiment Mode 1 can be preferably used as a substrate 510. In addition, a base film 511 and an amorphous semiconductor layer 512 are formed similarly to the embodiment 1. A solution containing a catalytic element of 5 to 100 ppm in terms of weight is applied by a spin coating method to form a layer 513 containing the catalytic element. Alternatively, the layer 513 containing the catalytic element may be formed by a sputtering method, an evaporation method, or the like. In that case, the thickness of the layer 513 containing the catalytic element is made 0.5 to 2 nm. The catalytic element is nickel (Ni), germanium (Ge), iron (Fe), palladium (Pd), tin (Sn), lead (Pb), cobalt (Co), platinum (Pt), copper (Cu), gold (Au) or the like.

[0039]

Thereafter, a heat treatment at 400 to 500°C for about 1 hour is first carried out, so that the hydrogen content of the amorphous semiconductor layer is made 5 atomic% or less. Then, a furnace for furnace annealing is used to carry out a thermal annealing in a nitrogen atmosphere at 550 to 600°C for 1 to 8 hours, preferably at 550°C for 4 hours. By the above steps, a crystalline semiconductor layer 514 made of a crystalline silicon film can be obtained (FIG. 7B). When the crystalline semiconductor layer fabricated by this heat annealing is macroscopically observed by an optical microscope, it is sometimes observed that an amorphous region locally remains. In such a case, according to the Raman spectroscopy, an amorphous component having a broad peak at 480 cm^{-1} is observed similarly. However, such an amorphous region can be easily removed by the dual beam laser annealing method of the present invention, and an excellent crystalline semiconductor layer can be obtained.

[0040]

As shown in FIG. 7C, an island-like semiconductor layer 515 is formed from the crystalline semiconductor layer 514. To the substrate in this state, as shown in FIG. 7D, the dual beam laser annealing is carried out similarly to Embodiment Mode 1. As a result, an island-like semiconductor layer 518 having a crystal structure is newly formed after a melting state is once formed by first laser light 516 and second laser light 517. As compared with the island-like semiconductor layer 507 explained in FIGS. 5A to 5C, in the island-like semiconductor layer 518 fabricated in this way, a crystal grain of a comparable size or larger size can be fabricated in the region A as the center. However, the catalytic element of about 1×10^{17} to 1×10^{19} $/cm^3$ is contained in the island-like semiconductor layer 518.

[0041]

[Embodiment Mode 3]

The crystallizing method of a semiconductor layer by the dual beam laser annealing method of the present invention is characterized in that the semiconductor layer formed into an island shape is made to have a temperature distribution, the region B rapidly cooled from the melted state and the region A in which the heat capacity of the under layer is large and which is gently cooled, are formed as explained in FIGS. 5 to 7, and a crystal of a large grain size is grown in the region A. Although the embodiment 1 and the embodiment 2 shows examples in which the thickness of the base film is changed to form the regions, such a structure can also be realized by using other methods.

[0042]

FIGS. 8A and 8B show an example of such methods. A heat conduction layer 521 made of tantalum (Ta), Ti, Cr, W, or the like and having a thickness of 50 to 100 nm is formed into an island shape on a substrate 520 of glass or the like set forth in Embodiment Mode 1. A base film 522 provided thereon is not subjected to an etching process, and an amorphous semiconductor layer 523 is laminated. After an island-like semiconductor layer is formed from the amorphous semiconductor layer 523, first laser light 524 and second laser light 525 are irradiated by the dual beam laser annealing method, so that a similar crystalline semiconductor layer 526 can be obtained. In the crystalline semiconductor layer 526, a region where the heat conduction layer 521 is formed corresponds to the region A, and the other portion corresponds to the region B.

[0043]

It is desirable that the heat conductivity of the heat conduction layer is 10 $Wm^{-1}K^{-1}$ or

higher. As such a material, an oxide of aluminum (aluminum oxide (Al_2O_3)) has a heat conductivity of 20 $Wm^{-1}K^{-1}$ and is suitable. The aluminum oxide is not limited to a stoichiometric ratio, but other elements may be added to control the heat conductivity characteristics and the characteristics of internal stress or the like. For example, nitrogen is made to be contained in aluminum oxide and aluminum nitride oxide (AlN_xO_{1-x}: $0.02 \leq x \leq 0.5$) may be used, or a nitride of aluminum (AlN_x) can also be used. Besides, a compound of silicon (Si), oxygen (O), nitrogen (N), and M (M is at least one selected from aluminum (Al) and rare earth elements) can be used. For example, AlSiON, LaSiON, or the like can be preferably used. In addition, boron nitride or the like can also be used. All the above oxide, nitride, and compounds can be formed by a sputtering method. This can be formed by using a target of desired composition and by using an inert gas such as argon (Ar) or nitrogen to perform sputtering.

[0044]

FIG. 9 shows an example in which instead of the heat conduction layer 521 of FIGS. 8A and 8B, a translucent heat conduction layer 527 containing an aluminum oxide film, an aluminum nitride film, or an aluminum nitride oxide film as its main ingredient is provided. When such a structure is made, and first laser light 528 and second laser light 529 are irradiated by the dual beam laser annealing method, a similar crystalline semiconductor layer 530 can be obtained. Also here, in the crystalline semiconductor layer 530, a region where the insulating layer 527 is formed corresponds to the region A, and the other portion corresponds to the region B.

[0045]

As described above, in this embodiment mode, although there has been described an example in which a method of using the temperature gradient of a semiconductor layer by providing the heat conduction layer under the base film is applied to the dual beam laser annealing method described in Embodiment Mode 1, such a method may be combined with Embodiment Mode 2 and is carried out.

[0046]

[Embodiment 1]

An example of the present invention will be described with reference to FIGS. 10A to 12B. Here, along steps, a description will be made on a method in which an n-channel TFT (hereinafter referred to as a pixel TFT) and a holding capacitor of a pixel portion, and an n-channel TFT and a p-channel TFT of a driving circuit provided at the periphery of the pixel portion are fabricated at the same time.

[0047]

In FIG. 10A, as a substrate 101, in addition to a glass substrate of barium borosilicate glass, alumino borosilicate glass, or the like typified by #7059 glass or #1737 glass of Corning Inc., in the case where a step of crystallization or activation is carried out by only a laser annealing method, a plastic substrate having no optical anisotropy, such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN), or polyethersulfone (PES), can be used. In the case where the glass substrate is used, a heat treatment may be previously carried out at a temperature lower than glass distortion point by about 10 to 20°C.

[0048]

Then, in order to prevent diffusion of an impurity from the substrate 101, a base film 102, such as a silicon oxide film, a silicon nitride film, or a silicon nitride oxide film, is formed on the

surface of the substrate where an island-like semiconductor layer as an active layer of a TFT is to be formed. For example, a silicon oxynitride film 102a of 10 to 100 nm formed by a plasma CVD method from SiH_4, NH_3, and N_2O and a hydrogenated silicon oxynitride film 102b of 100 to 200 nm similarly formed from SiH_4 and N_2O are laminated. Like this, although the base film 102 may be made a two-layer structure, one layer of the above materials may be formed, or a laminate structure of more than two layers may be formed. In any event, the film is formed to a thickness of about 100 to 300 nm.

[0049]

The silicon nitride oxide film is formed by using a conventional parallel plate type plasma CVD method. With respect to the silicon nitride oxide film 102a, SiH_4 of 10 SCCM, NH_3 of 100 SCCM, and N_2O of 20 SCCM were introduced into a reaction chamber, and substrate temperature of 325°C, reaction pressure of 40 Pa, discharge power density of 0.41 W/cm^2, discharge frequency of 60 MHz were used. On the other hand, with respect to the hydrogenated silicon oxynitride film 102b, SiH_4 of 5 SCCM, N_2O of 120 SCCM, and H_2 of 125 SCCM were introduced into the reaction chamber, and substrate temperature of 400°C, reaction pressure of 20 Pa, discharge power density of 0.41 W/cm^2, and discharge frequency of 60 MHz were used. These films can also be continuously formed by only changing the substrate temperature and switching the reaction gases. The silicon nitride oxide film 102a is formed so that the inner stress becomes tensile stress when the substrate is regarded as the center. Although the silicon oxynitride film 102b is also made to have the inner stress in the same direction, the stress in the absolute value is made smaller than that of the silicon nitride oxide film 102a.

[0050]

In order to form a thick portion and a thin portion in the base film 102, a resist mask is formed by a photolithography technique, and an etching process is carried out. Although a stepped portion is determined by the amount of etching, it is preferable to make the amount approximately 50 to 100 nm. For example, in order to etch the silicon oxynitride film 102b of 150 nm by 75 nm, a wet etching using a solution containing hydrofluoric acid may be used, or a dry etching using CF_4 or the like can be applied. In this way, a convex shape is formed in the base film 102, and the structure schematically shown in FIG. 10A is formed. At this time, although the size of the convex portion may be suitably determined in view of the size of a TFT to be fabricated, for the purpose of controlling the generation number of crystal nuclei, the size (diameter or length of a diagonal) of about 2 to 6 μm is preferable.

[0051]

Next, a semiconductor layer 103 having a thickness of 25 to 80 nm (preferably 30 to 60 nm) and an amorphous structure is formed by a method such as a plasma CVD method or a sputtering method. For example, the amorphous silicon film having a thickness of 55 nm is formed by the plasma CVD method. A semiconductor film having an amorphous structure includes an amorphous semiconductor layer and a microcrystalline semiconductor film, and a compound semiconductor film having an amorphous structure, such as an amorphous silicon germanium film or an amorphous silicon carbide film, may also be used.

[0052]

First, island-like semiconductor layers 104' to 108' having first shapes as shown in FIG. 10B are formed from the semiconductor layer 103 having the amorphous structure by a well-known

photolithography method. FIG. 13A is a top view of the island-like semiconductor layers 104' and 105' in this state, and similarly, FIG. 14A is a top view of the island-like semiconductor layer 108'. In FIGS. 13A to 13D and FIGS. 14A to 14D, although the island-like semiconductor layer is made rectangular and is formed so that one side has a length of 50 μm or less, the shape of the island-like semiconductor layer can be made arbitrary, and preferably, as long as the layer has such a shape that the minimum distance between its center and the end portion becomes 50 μm or less, any polygon or circle may be formed. Reference characters 102b-1 and 102b-2 of FIG. 13A and 102b-5 of FIG. 14A designate regions of convex portions of the base film 102 formed under the respective island-like semiconductor layers. This convex portion corresponds to the region A explained in Embodiments 1 to 3, and its periphery corresponds to the region B.

[0053]

Next, a crystallizing step is carried out to the island-like semiconductor layers 104' to 108' having such first shapes. As the crystallizing step, any method explained in Embodiments 1 and 2 can be applied. In any event, by applying the dual beam laser annealing method of the present invention, the island-like semiconductor layers 104' to 108' having the first shapes of FIG. 10B can be newly crystallized. In this case, the film is densified with the crystallization of the amorphous silicon film and is contracted by about 1 to 15%. Thus, it is conceivable that the island-like semiconductor layer made of such a crystalline silicon film has tensile stress when the substrate is regarded as the center.

[0054]

In the island-like semiconductor layer made of the crystalline semiconductor layer fabricated in this way, a large crystal grain is obtained mainly in the region of the convex portion, and a crystal grain becomes small in the vicinity of the end portion of the island-like semiconductor layer. Thus, the characteristics of the crystal become deteriorated, and even if a channel formation region of a TFT is formed in this portion, the characteristics of field effect mobility or the like become deteriorated.

[0055]

If a gate electrode of a TFT is formed to extend to the region having the poor characteristics of the crystal like this, excellent TFT characteristics can not be expected. Further, there is also a possibility that an off current value (value of current flowing in an off state of a TFT) is increased, or a current is concentrated in this region and heat is locally generated. Thus, as shown in FIGS. 13B and 14B, in order that the gate electrode does not extend to the end of the first shape island-like semiconductor layer, second shape island-like layers 104, 105 and 108 are formed. Regions 104', 105' and 108' indicated by dotted lines in the drawings indicate regions where the first shape island-like semiconductor layers existed, and are removed by etching so that the gate electrode does not overlap with at least the end portion of the region. The shape of the second shape island-like semiconductor layers 104, 105 and 108 may be made arbitrary. The other island-like semiconductor layers shown in FIG. 10B are also similarly treated.

[0056]

After the second shape island-like semiconductor layers 104 to 108 are formed, a mask layer 116 having a thickness of 50 to 100 nm and made of a silicon oxide film is formed to cover the island-like semiconductor layers 115 to 119 by the plasma CVD method or sputtering method. To the island-like semiconductor layers, for the purpose of controlling the threshold voltage (Vth) of a

TFT, an impurity to give a p type may be added at a concentration of about 1×10^{16} to 5×10^{17} atoms/cm^3 to all the surfaces of the island-like semiconductor layers. As an impurity to give the p type to a semiconductor, an element in group 13 of the periodic table, such as boron (B), aluminum (Al), or gallium (Ga), is known. Although an ion implantation method or ion doping method may be used as the method, the ion doping method is suitable for processing a large area substrate. In the ion doping method, diborane (B_2H_6) is used as a source gas, and boron (B) is added. Although injection of such an impurity element is not always necessary and may be omitted, it is a method preferably used especially for restricting the threshold voltage of an n-channel TFT within a predetermined range.

[0057]

In order to form an LDD region of the n-channel TFT of the driving circuit, an impurity element to give an n type is selectively added to the island-like semiconductor layers 105 and 107. For that purpose, resist masks 111 to 115 are formed in advance. As an impurity element to give the n type, phosphorus (P) or arsenic (As) may be used, and here, an ion doping method using phosphine (PH_3) is used to add phosphorus (P). In the present specification, impurity regions 117 and 118 formed here are called first low concentration n-type impurity regions, and the concentration of phosphorus (P) in this region is made within the range of 2×10^{16} to 5×10^{19} atoms/cm^3. The concentration is expressed by (n^-). An impurity region 119 is a semiconductor layer for forming holding capacity of a pixel matrix circuit, and phosphorus (P) with the same concentration is also added in this region (FIG. 10C).

[0058]

Next, a step of activating the added impurity element is carried out. Activation can be carried out by a heat treatment in a nitrogen atmosphere at 500 to 600°C for 1 to 4 hours, or a laser activation method. Both may be carried out at the same time. In the case of the method of the laser activation, a KrF excimer laser beam (wavelength of 248 nm) was used and a linear beam was formed, and under the conditions that the oscillation frequency was 5 to 50 Hz, the energy density was 100 to 500 mJ/cm^2, and the overlap ratio of the linear beam was 80 to 98%, scanning was made so that the entire surface of the substrate where the island-like semiconductor layers were formed was processed. Incidentally, irradiation conditions of the laser beam are not limited, but the user may appropriately determine. At this stage, the mask layer 116 is removed by etching using a solution of hydrofluoric acid or the like.

[0059]

In FIG. 10D, a gate insulating film 170 is formed of an insulating film having a thickness of 40 to 150 nm and containing silicon by using a plasma CVD method or a sputtering method. For example, a silicon nitride oxide film having a thickness of 120 nm is formed. Besides, in a silicon nitride oxide film formed by adding O_2 to SiH_4 and N_2O, a fixed charge density in the film is lowered, and it is a preferable material for this usage. Of course, the gate insulating film 170 is not limited to such a silicon nitride oxide film, but other insulating films containing silicon may be used as a single layer or a laminate structure. In any event, the gate insulating film 170 is formed to have compression stress when the substrate is regarded as the center.

[0060]

Then, as shown in FIG. 10D, a heat resistant conductive layer for forming a gate electrode is formed on the gate insulating film 170. Although the heat resistant conductive layer may be

formed of a single layer, a laminate structure made of plural layers, such as two layers or three layers, may be formed, as needed. It is appropriate that the heat resistant conductive material like this is used and such a structure is adopted that a conductive layer (A) 120 made of a conductive metal nitride film and a conductive layer (B) 121 made of a metal film are laminated. The conductive layer (B) 121 may be formed of an element selected from Ta, Ti, molybdenum (Mo), and W, or an alloy containing the foregoing element as its main ingredient, or an alloy film of a combination of the elements (typically Mo-W alloy film, Mo-Ta alloy film). The conductive layer (A) 120 is formed of tantalum nitride (TaN), WN, TiN, molybdenum nitride (MoN) or the like. Besides, the conductive layer (A) 120 may also be formed of tungsten silicide, titanium silicide, or molybdenum silicide. With respect to the conductive layer (B) 121, in order to lower the resistivity, it is preferable to decrease the concentration of the contained impurity, and especially, it was appropriate that the oxygen concentration was made 30 ppm or less. For example, with respect to W, when the oxygen concentration is made 30 ppm or less, a specific resistivity value of 20 μΩcm or less can be realized.

[0061]

It is appropriate that the thickness of the conductive layer (A) 120 is made 10 to 50 nm (preferably 20 to 30 nm), and the thickness of the conductive layer (B) 121 is made 200 to 400 nm (preferably 250 to 350 nm). In the case where the gate electrode is formed of the W film, the conductive layer (A) 120 is formed of a WN film having a thickness of 50 nm by a sputtering method using W as a target and introducing an argon (Ar) gas and a nitrogen (N_2) gas, and the conductive layer (B) 121 is formed of a W film having a thickness of 250 nm. As another method, the W film can also be formed by a thermal CVD method using tungsten hexafluoride (WF_6). In any event, in order to use it as the gate electrode, it is necessary to decrease the resistivity, and it is desirable to make the resistivity of the W film 20 μΩcm or less. Although the resistivity of the W film can be decreased by enlarging the crystal grain, in the case where many impurity elements such as oxygen are contained in the W film, crystallization is blocked and the resistivity is increased. As a result, in the case of the sputtering method, when a W target of purity of 99.9999% is used, and the W film is formed by sufficiently paying attention so that an impurity is not mixed from a vapor phase during the film formation, the resistivity of 9 to 20 μΩcm can be realized.

[0062]

On the other hand, in the case where a TaN film is used for the conductive layer (A) 120 and a Ta film is used for the conductive layer (B) 121, they can be formed similarly by the sputtering method. The TaN film is formed by using a target of Ta and a mixed gas of Ar and nitrogen as a sputtering gas, and the Ta film is formed by using Ar as the sputtering gas. If a suitable amount of Xe or Kr is added to the sputtering gas, the internal stress of the formed film is relieved, and peeling of the film can be prevented. The resistivity of α-phase Ta film is about 20 μΩcm and can be used for the gate electrode. However, the resistivity of β-phase Ta film is about 180 μΩcm and is not suitable for the gate electrode. Since the TaN film has a crystal structure close to the α-phase, if the Ta film is formed thereon, the α-phase Ta film can be easily obtained. Although not shown, it is effective to form a silicon film having a thickness of about 2 to 20 nm which is doped with phosphorus (P) under the conductive layer (A) 120. As a result, the improvement of adhesion of the conductive film formed thereon and prevention of oxidation are realized, and at the same time, it is possible to prevent a trace amount of alkali metal element

contained in the conductive layer (A) 120 or the conductive layer (B) 121 from diffusing. In any event, it is preferable that the resistivity of the conductive layer (B) 121 is made in the range of 10 to 50 μΩcm.

[0063]

Then, resist masks 122 to 127 are formed by using the photolithography technique, and the conductive layer (A) 120 and the conductive layer (B) 121 are simultaneously etched to form gate electrodes 128 to 132 and a capacitance wiring line 133. In the gate electrodes 128 to 132 and the capacitance wiring line 133, portions 128a to 132a made of the conductive layer (A) and portions 128b to 132b made of the conductive layer (B) are formed to be integrated (FIG. 11A). The positional relation among the island-like semiconductor layers 104 and 105 and the gate electrodes 128 and 129 in this state is shown in a top view of FIG. 13C. Similarly, the relation among the island-like semiconductor layer 108, the gate electrode 132, and the capacitance wiring line 133 is shown in FIG. 14C. In FIGS. 13C and 14C, the gate insulating film 170 is omitted.

[0064]

Although a method of etching the conductive layer (A) and the conductive layer (B) may be appropriately selected by the user, in the case where the layer is formed of a material containing W as its main ingredient as described above, it is desirable to use a dry etching method using high density plasma in order to carry out an etching at high speed and with high precision. As a method of obtaining the high density plasma, a microwave plasma or inductively coupled plasma (ICP) etching device may be used. For example, in the etching method of W using the ICP etching device, as an etching gas, two kinds of gases of CF_4 and Cl_2 are introduced in a reaction chamber, the pressure is made 0.5 to 1.5 Pa (preferably 1 Pa), and the high frequency (13.56 MHz) power of 200 to 1000 W is applied to an inductively coupled portion. At this time, the high frequency power of 20 W is applied to the stage where the substrate is placed, and it is charged at a negative potential by self-bias, so that a positive ion is accelerated and an anisotropic etching can be carried out. By using the ICP etching device, even the hard metal film of W or the like can also be etched at an etching rate of 2 to 5 nm/second. In order to carry out the etching without leaving the residue, it is appropriate that an etching time is increased at a ratio of about 10 to 20% to carry out over etching. However, at this time, it is necessary to pay attention to a selection ratio of etching to the under layer. For example, since the selection ratio of the silicon oxynitride film (gate insulating film 170) to the W film is 2.5 to 3, the surface where the silicon oxynitride film was exposed by such an over etching process, was etched by about 20 to 50 nm and became substantially thin.

[0065]

Then, in order to form an LDD region in the pixel TFT, a step of adding an impurity element to give an n type (n^- doping step) is carried out. Here, the impurity element to give the n type is added by an ion doping method using the gate electrodes 128 to 132 as masks in a self-aligned manner. The concentration of phosphorus (P) added as the impurity to give the n type is within the range of 1×10^{16} to 5×10^{19} /cm^3. In this way, as shown in FIG. 11B, second low concentration n-type impurity regions 134 to 137 are formed in the island-like semiconductor layers.

[0066]

Next, to the island-like semiconductor layers forming the n-channel TFTs, high concentration n-type impurity regions functioning as source regions or drain regions are formed (n^+

doping step). First, resist masks 138 to 141 are formed, and an impurity element to give the n type is added to form high concentration n-type impurity regions 142 to 147. Phosphorus (P) is used as the impurity element to give the n type in this region, and an ion doping method using phosphine (PH_3) is carried out so that its concentration becomes within the range of 1×10^{20} to 1×10^{21} /cm^3 (FIG. 11C).

[0067]

Then, in the island-like semiconductor layers 104 and 106 for forming the p-channel TFTs, high concentration p-type impurity regions 151 to 154 as source regions or drain regions are formed. Here, the gate electrodes 128 and 130 are used as masks, and an impurity element to give the p type is added to form the high concentration p-type impurity regions in a self-aligned manner. At this time, resist masks 148 to 150 are formed to cover all the surfaces of the island-like semiconductor films 105, 107, and 108 for forming the n-channel TFTs. The high concentration p-type impurity regions 151 to 154 are formed by an ion doping method using diborane (B_2H_6). The boron (B) concentration in this region is made 3×10^{20} to 3×10^{21} /cm^3 (FIG. 11D). In the high concentration p-type impurity regions 151 to 154, phosphorus (P) is added in the prior steps, and the high concentration p-type impurity regions 152 and 154 contain phosphorus at a concentration of 1×10^{20} to 1×10^{21} /cm^3, and the high concentration p-type impurity regions 151 and 153 contain phosphorus at a concentration of 1×10^{16} to 5×10^{19} /cm^3. However, since the concentration of boron (B) added in this step is made 1.5 to 3 times as high as that of phosphorus, no problem occurs in the function as the source region and drain region of the p-channel TFT.

[0068]

Thereafter, as shown in FIG. 12A, a first interlayer insulating film 155 is formed from gate electrodes and gate insulating films. The first interlayer insulating film may be formed of a silicon oxide film, a silicon oxynitride film, a silicon nitride film, or a laminate film of a combination of these. In any event, the first interlayer insulating film 155 is formed of an inorganic insulator material. The thickness of the first interlayer insulating film 155 is made 100 to 200 nm. Here, in the case where the silicon oxide film is used, the film can be formed by a plasma CVD method in which discharge is made under the conditions that tetraethyl ortho silicate (TEOS) and O_2 are mixed, the reaction pressure is made 40 Pa, the substrate temperature is made 300 to 400°C, and the high frequency (13. 56 MHz) power density is 0.5 to 0.8 W/cm^2. In the case where the silicon oxynitride film is used, the film may be formed of a silicon oxynitride film fabricated from SiH_4, N_2O, and NH_3 by the plasma CVD method, or a silicon oxynitride film fabricated from SiH_4 and N_2O. In this case, the film can be formed under fabricating conditions that the reaction pressure is 20 to 200 Pa, the substrate temperature is 300 to 400°C, and the high frequency (60 MHz) power density is 0.1 to 1.0 W/cm^2. Besides, a hydrogenated silicon oxynitride film fabricated from SiH_4, N_2O, and H_2 may be used. Similarly, the silicon nitride film can be fabricated from SiH_4 and NH_3 by the plasma CVD method. Such first interlayer insulating film is formed so as to have compression stress when the substrate is regarded as the center.

[0069]

Thereafter, a step of activating the impurity element to give the n type or p type, which was added at its own concentration, is carried out. This step is carried out by a thermal annealing method using an annealing furnace. In addition, a laser annealing method or a rapid thermal annealing method (RTA method) can be used. The thermal annealing method is carried out in a

nitrogen atmosphere containing oxygen at a concentration of 1 ppm or less, preferably 0.1 ppm or less, at 400 to 700°C, typically 500 to 600°C. In this embodiment, a heat treatment at 550°C for 4 hours was carried out. In the case where a plastic substrate with a low heat resisting temperature is used as the substrate 101, it is preferable to use the laser annealing method.

[0070]

After the step of activation, further, a heat treatment at 300 to 450°C for 1 to 12 hours is carried out in an atmosphere containing hydrogen of 3 to 100%, and a step of hydrogenating the second shape island-like semiconductor layer is carried out. This step is a step of terminating dangling bonds of 10^{16} to $10^{18}/cm^3$ existing in the second shape island-like semiconductor layer by thermally excited hydrogen. As another means of hydrogenation, plasma hydrogenation (using hydrogen excited by plasma) may be carried out. Besides, by a heat treatment at 300 to 450°C, the island-like semiconductor layer may be hydrogenated by diffusing hydrogen of the hydrogenated silicon oxynitride film of the base film 102 and the silicon oxynitride film of the first interlayer insulating film 155.

[0071]

After the steps of activation and hydrogenating are ended, a second interlayer insulating film 156 made of an organic insulating material is formed to an average thickness of 1.0 to 2.0 μm. As the organic resin material, polyimide, acrylic, polyamide, polyimide amid, BCB (benzocyclobutene), or the like can be used. For example, in the case where polyimide of a type which is thermally polymerized after application onto a substrate is used, a clean oven is used and sintering is made at 300°C to form the film. In the case where acrylic is used, a two-liquid type is used, and after a main material and a hardening agent are mixed, a spinner is used to apply it onto the entire surface of a substrate, and then, preheating at 80°C for 60 seconds is carried out by a hot plate. Further, a clean oven is used and sintering at 250°C for 60 minutes is carried out to form the film.

[0072]

The second interlayer insulating film is formed of the organic insulator material, so that the surface can be excellently flattened. Besides, since the organic resin material has generally a low dielectric constant, parasitic capacitance can be lowered. However, since it has a hygroscopic property and is not suitable for a protecting film, as in this embodiment, it is necessary to use the material in combination with the silicon oxide film, silicon oxynitride film, silicon nitride film, or the like formed as the first insulating film 155.

[0073]

Thereafter, a photomask is used to form a resist mask of a predetermined pattern, and contact holes reaching source regions or drain regions formed in the respective island-like semiconductor films are formed. The contact holes are formed by a dry etching method. In this case, a mixed gas of CF_4, O_2, and He is used as an etching gas, and the second interlayer insulating film 156 made of the organic resin material is first etched, and thereafter, CF_4 and O_2 are used as an etching gas, and the first insulating film 155 is etched. Further, in order to raise the selection ratio to the island-like semiconductor layer, an etching gas is changed to CHF_3 to etch the gate insulating film 170, so that the contact holes can be excellently formed.

[0074]

Then, a conductive metal film is formed by a sputtering method or a vacuum evaporation

method, a resist mask pattern is formed, and source wiring lines 157 to 161 and drain wiring lines 162 and 166 are formed by etching. A drain wiring line 167 indicates a drain wiring line of an adjacent pixel. Here, the drain wiring line 166 functions as a pixel electrode. Although not shown, in this example, this electrode is wired in such a manner that a Ti film having a thickness of 50 to 150 nm is formed, a contact to the semiconductor film forming the source or drain region of the island-like semiconductor layer is formed, and aluminum (Al) having a thickness of 300 to 400 nm is formed to overlap with the Ti film.

[0075]

FIG. 13D is a top view showing, in this state, the island-like semiconductor layers 104 and 105, the gate electrodes 128 and 129, the source wiring lines 157 and 158, and the drain wiring lines 162 and 163. The source wiring lines 157 and 158 are connected to the island-like semiconductor layers 104 and 105 at portions 230 and 233 through not-shown contact holes provided in the second interlayer insulating film and the first interlayer insulating film, respectively. The drain wiring line 162 and 163 are connected to the island-like semiconductor layers 104 and 105 at portions 231 and 232, respectively. Similarly, FIG. 14D is a top view showing the island-like semiconductor layer 108, the gate electrode 132, the capacitance wiring line 133, the source wiring line 161, and the drain wiring line 166. The source wiring line 161 and the drain wiring line 166 are connected through a contact portion 234 and a contact portion 235 to the island-like semiconductor layer 108, respectively.

[0076]

In this state, a heat treatment is carried out to improve contact of the contact portions between the source wiring lines 157 to 161, the drain wiring lines 162 to 166 and their respective island-like semiconductor layers. The heat treatment is carried out by using a clean oven and within the range of 200 to 300°C for 1 to 4 hours.

[0077]

In this way, the substrate including the TFTs of the driving circuit and the pixel TFT of the pixel portion on the same substrate can be completed. In the driving circuit, a first p-channel TFT 200, a first n-channel TFT 201, a second p-channel TFT 202, and a second n-channel TFT 203 are formed. In the pixel portion, a pixel TFT 204 and a holding capacitor 205 are formed. In the present specification, for convenience, such a substrate is called an active matrix substrate.

[0078]

The first p-channel TFT 200 of the driving circuit has a single drain structure including, in the second shape island-like semiconductor film 104, a channel formation region 206, source regions 207a and 207b, and drain regions 208a and 208b, which are made of high concentration p-type impurity regions. The first n-channel TFT 201 includes, in the second shape island-like semiconductor film 105, a channel formation region 209, an LDD region 210 overlapping with the gate electrode 129, a source region 212, and a drain region 211. In this LDD region, the LDD region overlapping with the gate electrode 129 is designated as Lov, and its length in the channel length direction was made 0.5 to 3.0 μm, preferably 1.0 to 2.0 μm. By setting the length of the LDD region in the n-channel TFT in this way, a high electric field generated in the vicinity of the drain region is relieved, generation of a hot carrier is prevented, and deterioration of the TFT can be prevented. Similarly, the second p-channel TFT 202 of the driving circuit has a single drain structure including, in the second shape island-like semiconductor film 106, a channel formation

region 213, source regions 214a and 214b, and drain regions 215a and 215b, which are made of high concentration p-type impurity regions. The second n-channel TFT 203 includes, in the second shape island-like semiconductor film 107, a channel formation region 216, LDD regions 217 and 218 partially overlapping with the gate electrode 131, a source region 220, and a drain region 219. The length of the region Lov overlapping with the gate electrode 131 of the TFT was also made 0.5 to 3.0 μm, preferably 1.0 to 2.0 μm. The LDD region which is not overlapping with the gate electrode 131 is designated as Loff, and its length in the channel length direction was made 0.5 to 4.0 μm, preferably 1.0 to 2.0 μm. The pixel TFT 204 includes, in the island-like semiconductor film 108, channel formation regions 221 and 222, LDD regions 223 to 225, and source or drain regions 226 to 228. The length of the LDD region (Loff) in the channel length direction is 0.5 to 4.0 μm, preferably 1.5 to 2.5 μm. Further, the holding capacitor 205 is formed of the capacitance wiring line 133, an insulating film made of the same material as the gate insulating film, and a semiconductor layer 229 connecting with the drain region 228 of the pixel TFT 204. In FIG. 12B, although the pixel TFT 204 is made to have a double gate structure, a single gate structure may be adopted, or a multi-gate structure in which a plurality of gate electrodes are provided may be adopted.

[0079]

FIG. 15 is a top view showing substantially one pixel of the pixel portion of such an active matrix substrate. A section taken along A-A' in the drawing corresponds to the sectional view of the pixel portion shown in FIG. 12B. In the pixel TFT 204, the gate electrode 132 serving also as the gate wiring line intersects with the under island-like semiconductor layer 108 through a not-shown gate insulating film. Although not shown, the source region, the drain region, and the LDD region are formed in the island-like semiconductor layer. Reference numeral 234 designates a contact portion between the source wiring line 161 and the source region 226, 235 designates a contact portion between the drain wiring line 166 and the drain region 228. The holding capacitor 205 is formed at a region where the semiconductor layer 229 extending from the drain region 228 of the pixel TFT 204 overlaps with the capacitance wiring line 133 through the gate insulating film.

[0080]

The second shape island-like semiconductor layer formed through the foregoing steps by the dual beam laser annealing method of the present invention has such a structure that the size of a crystal grain is enlarged especially in the channel formation region and grain boundaries are few. The second shape island-like semiconductor layer like this is used, and the structures of the pixel TFT and the TFTs constituting each circuit are optimized in accordance with the specification required by the driving circuit, so that it becomes possible to improve the operation performance and reliability of the semiconductor device. Further, activation of the LDD region, the source region and the drain region is facilitated by forming the gate electrode out of the conductive material having heat resistance. Then, a high quality display device can be realized by such an active matrix substrate. From the active matrix substrate fabricated in this example, a reflection type liquid crystal display device can be fabricated.

[0081]

[Embodiment 2]

The active matrix substrate fabricated in Embodiment 1 can be directly used for a reflection type liquid crystal display device. On the other hand, in the case of forming a

transmission type liquid crystal display device, it is sufficient if a pixel electrode provided for each pixel of a pixel portion is formed of a transparent electrode. In this example, a method of fabricating an active matrix substrate corresponding to the transmission type liquid crystal display device will be described with reference to FIGS. 16A and 16B.

[0082]

The active matrix substrate is fabricated similarly to Embodiment 1. FIG. 16 shows a structure of a pixel portion thereof. FIG. 16A shows an example in which a transparent conductive film is first formed on a second interlayer insulating film, a patterning process and an etching process are carried out to form a pixel electrode 171, and then, a drain wiring line 172 is formed to partially overlap with the pixel electrode 171. As shown in FIG. 16B, a Ti film 172a is formed to a thickness of 50 to 150 nm, a semiconductor film for forming a source or drain region of an island-like semiconductor layer and a contact are formed, and an Al film 172b having a thickness of 300 to 400 nm is formed on the Ti film 172a. When this structure is adopted, the pixel electrode 171 is in contact with only the Ti film 172a forming the drain wiring line 172. As a result, it is possible to certainly prevent the transparent conductive material from directly coming in contact with and reacting with Al.

[0083]

As a material of the transparent conductive film, it is possible to use indium oxide (In_2O_3), indium oxide-tin oxide alloy (In_2O_3-SnO_2; ITO), or the like, which is formed by a sputtering method or a vacuum evaporation method. An etching process of such material is carried out by a hydrochloric acid base solution. However, etching of ITO is especially liable to generate the residue, and in order to improve the etching workability, indium oxide-zinc oxide alloy (In_2O_3-ZnO) may be used. The indium oxide-zinc oxide alloy has features that it are excellent in surface flatness and is also excellent in heat stability as compared with ITO. Similarly, zinc oxide (ZnO) is also a suitable material, and further, in order to raise transmissivity of visible light and conductivity, zinc oxide (ZnO: Ga) to which gallium (Ga) is added, or the like can be used.

[0084]

The structure of the driving circuit may be the same as Embodiment 1, and in this way, the active matrix substrate corresponding to the transmission type display device can be completed.

[0085]

[Embodiment 3]

In a method of fabricating an island-like semiconductor layer having a crystal structure from an island-like semiconductor layer having an amorphous structure by the dual beam laser annealing method of the present invention, a trace amount (about 1×10^{17} to 1×10^{19} /cm^3) of catalytic element used for crystallization remains in the island-like semiconductor layer having the crystal structure fabricated by the method of Embodiment 2. Of course, although a TFT can be completed even in such a state, it is preferable to remove the remaining catalytic element from at least a channel formation region. As one of the ways for removing this catalytic element, there is a way to use the gettering function of phosphorus (P).

[0086]

A gettering process by phosphorus (P) for this object can be carried out in parallel with the activation step explained in FIG. 12A. This state will be described with reference to FIG. 17. The concentration of phosphorus (P) required for gettering may be comparable to the impurity

concentration of the high concentration n-type impurity region, and by the thermal annealing of the activation step, the catalytic element can be made to segregate from the channel formation regions of the n-channel TFT and the p-channel TFT through the concentration into the impurity regions containing phosphorus (P) (directions of arrows shown in FIG. 17). As a result, the catalytic element segregates in the impurity region, and the concentration becomes about 1×10^{17} to 1×10^{19} atoms/cm^3. In the TFT fabricated in this way, its off current value is lowered and crystallinity is excellent, so that high field effect mobility can be obtained and excellent characteristics can be achieved.

[0087]

[Embodiment 4]

In this embodiment, a process of fabricating an active matrix type liquid crystal display device from an active matrix substrate fabricated in Embodiment 1 will be described. As shown in FIG. 18, columnar spacers 901 and 902 are formed on the active matrix substrate in the state of FIG. 12B. Although a method of dispersing particles of several μm to provide the spacers may be used, the columnar spacers may be formed like this by forming a resin film on the entire surface of the substrate and patterning this. Although the material of such columnar spacers is not restricted, for example, NN700 made by JSR Co., Ltd. is used, and after it is applied by a spinner, an exposure and a developing process are carried out to form a predetermined pattern. Further, heating at 150 to 200°C is carried out by a clean oven or the like to harden it. Although the shape of the columnar spacer fabricated in this way can be changed by conditions of the exposure and developing process, if the shape of each of the columnar spacers 901 and 902 is preferably made such that it is columnar and its top is flat, it is suitable in securing the mechanical strength as a liquid crystal display panel when an opposite side substrate is fitted. Although the shape of the columnar spacer may be cylindrical or prismatic and is not particularly limited, for example, when it is cylindrical, specifically, the height H is made 1.2 to 5 μm, the average radius L1 is made 5 to 7 μm, and the ratio of the average radius L1 to the radius L2 of the bottom portion is made 1 : 1.5. At this time, a taper angle of a side is made ±15E or less.

[0088]

Although the arrangement of the columnar spacers may be arbitrarily determined, preferably, as shown in FIG. 18, in the pixel portion, the columnar spacer 902 is formed to overlap with the contact portion 235 of the drain wiring line 166 (pixel electrode) to cover the portion. Since the flatness of the contact portion 235 is damaged and liquid crystal comes not to be oriented well in this portion, when the columnar spacer 902 is formed in the form of filling the contact portion 235 with the resin for the spacer in this way, disclination or the like can be prevented.

[0089]

Thereafter, an oriented film 903 is formed. Normally, polyimide resin is used for an oriented film of a liquid crystal display device. After the oriented film is formed, a rubbing treatment is carried out so that liquid crystal molecules are oriented with a certain constant pretilt angle. The rubbing treatment is carried out so that a region which is not subjected to rubbing in the rubbing direction from the end portion of the columnar spacer 902 provided in the pixel portion becomes 2 μm or less. Although generation of static electricity often becomes a problem in the rubbing treatment, when the columnar spacer 901 is formed on the TFT of the driving circuit and to cover the source wiring line and the drain wiring line, the original role of the spacer and the effect to

protect the TFT from the static electricity in the rubbing step can be obtained. In FIG. 18, although the columnar spacers 901 are dividedly formed on the source wiring line and the drain wiring line on the TFT of the driving circuit, in addition, they may be formed to cover the entire surface of the driving circuit.

[0090]

A light shielding film 905, a transparent conductive film 906, and an oriented film 907 are formed on an opposite substrate 904 at the opposite side. The light shielding film 905 is formed of Ti, Cr, Al or the like to a thickness of 150 to 300 nm. The active matrix substrate in which the pixel portion and the driving circuit are formed is bonded to the opposite substrate through a sealing agent 908. A filler 909 is mixed in the sealing agent 908, and the two substrates are bonded while a uniform interval is kept by the filler 909 and the columnar spacers 901 and 902. Thereafter, a liquid crystal material 910 is injected between both the substrates, and complete sealing is made by a sealing agent (not shown). As the liquid crystal material, a well-known liquid crystal material may be used. For example, in addition to a TN liquid crystal, it is also possible to use a thresholdless antiferroelectric mixed liquid crystal showing electro-optical response properties in which transmissivity is continuously changed to an electric field. Some thresholdless antiferroelectric mixed liquid crystal shows V-shaped electro-optical response characteristics. In this way, the active matrix type liquid crystal display device shown in FIG. 18 is completed.

[0091]

FIG. 19 is a top view of an active matrix substrate, which shows the positional relation of a pixel portion, a driving circuit portion, a spacer and a sealing agent. A scan signal driving circuit 701 and an image signal driving circuit 702 are provided as driving circuits at the periphery of a pixel portion 700. Further, a signal processing circuit 703 such as a CPU or a memory may be added. These driving circuits are connected to an external input/output terminal 710 through a connection wiring line 711. In the pixel portion 700, a gate wiring line group 704 extending from the scan signal driving circuit 701 and a source wiring line group 705 extending from the image signal driving circuit 702 intersect with each other in matrix form to shape pixels, and a pixel TFT 204 and a holding capacitor 205 are provided in each pixel.

[0092]

The columnar spacer 706 provided in the pixel portion corresponds to the columnar spacer 902 shown in FIG. 18. Although the spacer may be provided for every pixel, it may be provided every several to several tens pixels arranged in matrix form. That is, it is appropriate that the ratio of the number of spacers to the total number of pixels constituting the pixel portion is made 20 to 100%. Spacers 707, 708, and 709 provided at the driving circuit portion may be provided to cover the entire surface, or may be provided so that they are divided into plural portions in conformity with the position of the source and drain wiring line of each TFT as shown in FIG. 18.

[0093]

A sealing agent 714 is formed outside of the pixel portion 700 on the substrate 101, the scan signal driving circuit 701, the image signal driving circuit 702, and the other signal processing circuit 703, and inside of the external input/output terminal 710.

[0094]

The structure of such an active matrix type liquid crystal display device will be described with reference to a perspective view of FIG. 20. In FIG. 20, the active matrix substrate is constituted by the pixel portion 700, the scan signal driving circuit 701, the image signal driving

circuit 702, and the other signal processing circuit 703, which are formed on the glass substrate 101. In the pixel portion 700, the pixel TFT 204 and the holding capacitor 205 are provided, and the driving circuits provided at the periphery of the pixel portion are constituted with a CMOS circuit as a base. The scan signal driving circuit 701 and the image signal driving circuit 702 are connected to the pixel TFT 204 through the gate wiring line 132 and the source wiring line 161, respectively. A flexible printed circuit (FPC) 713 is connected to the external input terminal 710 and is used to input an image signal or the like. The flexible printed circuit 713 is fixed while the adhesion strength is raised by a reinforcing resin 712, and is connected to the respective driving circuits through the connection wiring line 711. Although not shown, a light shielding film and a transparent electrode are provided on an opposite substrate 175.

[0095]

The liquid crystal display device of such a structure can be formed by using the active matrix substrate shown in Embodiments 1 to 3. For example, when the active matrix substrate shown in Embodiment 1 is used, a reflection type liquid crystal display device can be obtained, and when the active matrix substrate shown in Embodiment 2 is used, a transmission type liquid crystal display device can be obtained.

[0096]

[Embodiment 5]

In this embodiment, with reference to FIG. 21, a description will be made on an example in which the present invention is applied to a display device (organic EL display device) using an active matrix type organic electroluminescence (organic EL) material. FIG. 21A is a circuit diagram of an active matrix type organic display device in which a display region and a driving circuit at the periphery thereof are provided on a glass substrate. This organic EL display device is constituted by a display region 11, an X-direction peripheral driving circuit 12, and a Y-direction peripheral driving circuit 13, which are provided on the substrate. This display region 11 is constituted by a switching TFT 30, a holding capacitor 32, a current controlling TFT 31, an organic EL element 33, X-direction signal lines 18a and 18b, power source lines 19a and 19b, and Y-direction signal lines 20a, 20b and 20c, and the like.

[0097]

FIG. 21B is a top view showing substantially one pixel. It is appropriate that the switching TFT 30 is formed in the same way as the n-channel TFT 204 shown in FIG. 10C, and the current controlling TFT 31 is formed in the same way as the n-channel TFT 201.

[0098]

FIG. 22 is a sectional view taken along line B-B' of FIG. 21B, which shows the switching TFT 30, the holding capacitor 32, the current controlling TFT 31, and an organic EL element portion. In FIG. 22, island-like semiconductor layers 43 and 44 are fabricated by the method of Embodiments 1 to 4. Then, base films 41 and 42, a gate insulating film 45, a first interlayer insulating film 46, gate electrodes 47 and 48, a capacitance wiring line 49, source and drain wiring lines 18a, 19a, 51, 52, and a second interlayer insulating film 50 are fabricated on a substrate 40 in the same way as Embodiment 1. Then, similarly to the second interlayer insulating film 50, a third interlayer insulating film 53 is formed thereon, and after a contact hole reaching the drain wiring line 52 is formed, a pixel electrode 54 made of a transparent conductive film is formed. The organic EL element portion is formed of the pixel electrode 54, an organic EL layer 55 formed over

the pixel electrode and the third interlayer insulating film 53, a first electrode 56 formed on the organic EL layer 55 and made of MgAg compound, and a second electrode 57 made of Al. Although not shown, if a color filter is provided, color display can also be performed. In any event, if the method of fabricating the active matrix substrate shown in the Embodiments 1 to 5 is applied, the active matrix type EL display device can be easily fabricated.

[0099]

[Embodiment 6]

An active matrix substrate, a liquid crystal display device, and an EL display device fabricated by carrying out the present invention can be used for various electro-optical devices. Further, the present invention can be applied to all electronic instruments incorporating such electro-optical devices as display media. As the electronic instrument, a personal computer, a digital camera, a video camera, a portable information terminal (mobile computer, portable telephone, electronic book, etc.), a navigation system, and the like can be enumerated.

[0100]

FIG. 23A shows a portable information terminal which is constituted by a main body 2201, an image input portion 2202, an image receiving portion 2203, an operation switch 2204, and a display device 2205. The present invention can be applied to the display device 2205 and other signal control circuits.

[0101]

Such a portable information terminal is often used outdoors as well as indoors. In order to enable a long time use, a reflection type liquid crystal display device which does not use a backlight but uses outer light is suitable as a low power consumption type. However, in the case where the environment is dark, a transmission type liquid crystal display device provided with a backlight is suitable. From such a background, a hybrid liquid crystal display device provided with characteristics of both the reflection type and the transmission type has been developed. The present invention can also be applied to such a hybrid liquid crystal display device. The display device 2205 is constituted by a touch panel 3002, a liquid crystal display device 3003, and an LED backlight 3004. The touch panel 3002 is provided to facilitate the operation of the portable information terminal. In the structure of the touch panel 3002, a light emitting element 3100 such as an LED is provided at one end, a light receiving element 3200 such as a photodiode is provided at the other end, and an optical path is formed therebetween. When this touch panel 3002 is pressed to block the light path, the output of the light receiving element 3200 is changed. Thus, when this principle is used and the light emitting element and the light receiving element are arranged in matrix form on the liquid crystal display device, the panel can be made to function as an input medium.

[0102]

FIG. 23B shows a structure of a pixel portion of a hybrid liquid crystal display device. A drain wiring line 177 and a pixel electrode 178 are provided on an interlayer insulating film on the pixel TFT 204 and the holding capacitor 205. Such a structure can be formed by applying Embodiment 4. The drain wiring line is made of a laminate structure of a Ti film and an Al film, and is made a structure serving also as a pixel electrode. The pixel electrode 177 is formed by using a transparent conductive film material explained in Embodiment 4. When the liquid crystal display device 3003 is fabricated from such an active matrix substrate, it can be preferably used for

a portable information terminal.

[0103]

FIG. 24A shows a personal computer which is constituted by a main body 2001 provided with a microprocessor, a memory and the like, an image input portion 2002, a display device 2003, and a keyboard 2004. The present invention can be applied to the display device 2003 and other signal processing circuits.

[0104]

FIG. 24B shows a video camera which is constituted by a main body 2101, a display device 2102, an audio input portion 2103, operation switches 2104, a battery 2105, and an image receiving portion 2106. The present invention can be applied to the display device 2102 and other signal control circuits.

[0105]

FIG. 24B shows a goggle type display which is constituted by a main body 2901, a display device 2902, and an arm portion 2903. The present invention can be applied to the display device 2902 and other not-shown signal control circuits.

[0106]

FIG. 24D shows an electronic game machine, such as a TV game or a video game, which is constituted by an electronic circuit 2308 such as a CPU, a main body 2301 mounted with a recording medium 2304 or the like, a controller 2305, a display device 2303, and a display device 2302 incorporated in the main body 2301. The display device 2303 and the display device 2302 incorporated in the main body 2301 may display the same information. Alternatively, the former is made a main display device, and the latter is made a sub display device which displays information of the recording medium 2304, displays the operation state of the machine, or can also be made an operation plate by adding the function of a touch sensor. Besides, the main body 2301, the controller 2305, and the display device 2303 may be connected through wired communication to mutually transmit signals, or may be connected through wireless communication or optical communication by providing sensor portions 2306 and 2307. The present invention can be applied to the display devices 2302 and 2303. A conventional CRT may be used for the display device 2303.

[0107]

FIG. 24D shows a player using a recording medium storing a program (hereinafter referred to as a "recording medium"), which is constituted by a main body 2401, a display device 2402, a speaker portion 2403, a recording medium 2404, and an operation switch 2405. A DVD (Digital Versatile Disc), compact-disc (CD), or the like is used as the recording medium, and reproduction of a music program, picture display, information display through a video game (or TV game) or the Internet can be performed. The present invention can be preferably applied to the display device 2402 and other signal control circuits

[0108]

FIG. 24E shows a digital camera which is constituted by a main body 2501, a display device 2502, an eyepiece portion 2503, operation switches 2504, and an image receiving portion (not shown). The present invention can be applied to the display device 2502 and other signal control circuits.

[0109]

FIG. 25A shows a front type projector which is constituted by an optical source system and a display device 2601 and a screen 2602. The present invention can be applied to the display device and other signal control circuits. FIG. 25B shows a rear type projector which is constituted by a main body 2701, an optical source system and display device 2702, a mirror 2703, and a screen 2704. The present invention can be applied to the display device and other signal control circuits.

[0110]

FIG. 25C is a view showing an example of the structures of the light source optical system and display devices 2601 and 2701 in FIG. 25A and FIG. 25B. Each of the light source optical system and display devices 2601 and 2702 is constituted by a light source optical system 2801, mirrors 2802, and 2804 to 2806, a dichroic mirror 2803, a beam splitter 2807, a liquid crystal display device 2808, a phase difference plate 2809, and a projection optical system 2810. The projection optical system 2810 is constituted by a plurality of optical lenses. Although FIG. 25C shows an example of a three-plate system in which three liquid crystal display devices 2808 are used, the invention is not limited to this system, but a single plate optical system may be adopted. Besides, in light paths indicated by arrows in FIG. 25C, an optical lens, a film having a polarizing function, a film for adjusting a phase, an IR film or the like may be suitably provided. FIG. 25D is a view showing an example of the structure of the light source optical system 2801 in FIG. 25C. In this embodiment, the light source optical system 2801 is constituted by a reflector 2811, a light source 2812, lens arrays 2813 and 2814, a polarization conversion element 2815, and a condensing lens 2816. Incidentally, the light source optical system shown in FIG. 25D is merely an example, and the invention is not limited to the structure shown in the drawing.

[0111]

Besides, although not shown here, the present invention can also be applied to a navigation system, a readout circuit of an image sensor, and so on. In this manner, the scope of application of the present invention is very wide, and the invention can be applied to electronic instruments of any fields. Besides, the electronic instruments of this embodiment can be realized by using the techniques of Embodiments 1 to 5.

[Brief Description of Drawings]

[FIG. 1] A view for explaining the concept of a laser annealing method of the present invention.

[FIG. 2] Views for explaining a structure of a laser annealing apparatus.

[FIG. 3] Views for explaining a structure of an optical system of the laser annealing apparatus.

[FIG. 4] A view for explaining a structure of an optical system of a laser annealing apparatus.

[FIG. 5] Views for explaining a fabricating process of an island-like semiconductor layer of the present invention.

[FIG. 6] A view for explaining the concept of crystallization of the present invention.

[FIG. 7] Views for explaining a fabricating process of an island-like semiconductor layer of the present invention.

[FIG. 8] Views for explaining the fabricating process of the island-like semiconductor layer of the present invention.

[FIG. 9] A view for explaining the fabricating process of the island-like semiconductor layer of the present invention.

[FIG. 10] Sectional views for explaining a fabricating process of a pixel TFT and TFTs of a driving circuit.

[FIG. 11] Sectional views for explaining the fabricating process of the pixel TFT and the TFTs of the driving circuit.

[FIG. 12] Views for explaining the fabricating process of the pixel TFT and the TFTs of the driving circuit.

[FIG. 13] Top views showing a fabricating process of a TFT of a driving circuit.

[FIG. 14] Top views showing a fabricating process of a pixel TFT.

[FIG. 15] A top view showing a pixel structure of a pixel portion.

[FIG. 16] Sectional views sowing a structure of a pixel TFT.

[FIG. 17] A sectional view showing a fabricating process of a pixel TFT and TFTs of a driver circuit.

[FIG. 18] A sectional view of an active matrix type liquid crystal display device.

[FIG. 19] A top view for explaining an input/output terminal, a wiring line, a circuit arrangement, a spacer, and an arrangement of a sealing agent in a liquid crystal display device.

[FIG. 20] A perspective view showing a structure of a liquid crystal display device.

[FIG. 21] Views showing a structure of an active matrix type EL display device.

[FIG. 22] A sectional view showing a structure of a pixel portion of an active matrix type EL display device.

[FIG. 23] Views showing an example of a semiconductor device.

[FIG. 24] Views showing examples of semiconductor devices.

[FIG. 25] Views showing structures of projection type liquid crystal display devices.

[Name of Document] Abstract
[Summary]
[Problem] A crystalline semiconductor film in which the position and size of a crystal grain is controlled is fabricated, and the crystalline semiconductor film is used for a channel formation region of a TFT, so that a high performance TFT is realized.
[Solving Means] An island-like semiconductor layer is made to have a temperature distribution, and a region where temperature change is gentle is provided to control the nucleus generation speed and nucleus generation density, so that the crystal grain is enlarged. In a region where an island-like semiconductor layer 1003 overlaps with a base film 1002, a thick portion is formed in the base film 1002. The volume of this portion increases and heat capacity becomes large, so that a cycle of temperature change by irradiation of a pulse laser beam to the island-like semiconductor layer becomes gentle (as compared with other thin portion). In this manner, a laser beam is irradiated from the front side and reverse side of the substrate to directly heat the semiconductor layer, and heat conduction from the semiconductor layer to the side of the substrate and heat conduction of the semiconductor layer in the horizontal direction to the substrate are used, so that the increase in the size of the crystal grain is realized.
[Selected drawing] FIG. 1